The opinion in support of the decision being entered today was <u>not</u> written for publication and is <u>not</u> binding precedent of the Board.

Paper No. 30

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UNITED STATES PATENT AND TRADEMARK OFFICE

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PAT. & T.M. OFFICE ARD OF PATENT APPEAL AND INTERFERENCES BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte BRENT KEETH and PIERRE C. FAZAN

Appeal No. 2000-0556 Application No. 08/530,661

HEARD: January 22, 2002

Before RUGGIERO, DIXON, and LEVY, <u>Administrative Patent Judges</u>.

LEVY, <u>Administrative Patent Judge</u>.

### DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 6-10, 18, 19, 22, 23, 25, and 26. Claims 1-5, 11-17, 20, 21, 24, and 27 have been withdrawn from consideration.

### BACKGROUND

Appellants' invention relates to a semiconductor memory device. An understanding of the invention can be derived from a reading of exemplary claim 22, which is reproduced as follows:

# 22. A semiconductor memory device comprising:

a total of no more than 68,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on a semiconductor die, and circuitry formed on the semiconductor die permitting data to be written to and read from one or more of the memory cells, at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area having at least 128 of the functional and operably addressable memory cells.

The prior art reference of record relied upon by the examiner in rejecting the appealed claims is:

Denboer, A. "Inside Today's Leading Edge Microprocessors" Semiconductor International, Feb. 1994.

Claims  $6-10^1$ , 18, 19, 22, 23, 25, and 26 stand rejected under 35 U.S.C. § 112, first paragraph, based upon lack of enablement.

Claims 6-10, 18, 19, 22, 23, 25, and 26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Admitted Prior Art in view of Denboer.

Rather than reiterate the conflicting viewpoints advanced by the examiner and appellants regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 26, mailed December 16, 1999) for the examiner's complete reasoning in

The examiner only lists claims 6-8. However, we consider claims 9 and 10 to be included because the examiner refers, in the rejection (answer, page 3), to limitations found in these claims. Appellants likewise consider claims 9 and 10 to be considered in the rejection (brief, page 3).

support of the rejections, and to appellants' brief (Paper No. 25, filed November 12, 1999) for appellants' arguments thereagainst. Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the brief have not been considered. See 37 CFR 1.192(a).

## OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the rejections advanced by the examiner, and the evidence relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, appellants' arguments set forth in the brief along with the examiner's rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer. Upon consideration of the record before us, we reverse.

We begin with the rejection of claims 6-10, 18, 19, 22, 23, 25, and 26 under 35 U.S.C. § 112, first paragraph. Appellant asserts (brief, page 6) that:

[T]he Examiner's rejection on grounds that the enablement is not commensurate with the scope of the claims is based on the incorrect legal premise that a generic claim cannot literally

cover species that are not disclosed and may go beyond the ability of a person of ordinary skill in the art given appellants' specification at the time of filing of the patent application.

Appellants further assert (<u>id.</u>) that "[t]he scope of enablement need only bear a 'reasonable correlation' to the scope of the claims as of the filing date." Appellants additionally assert (<u>id.</u>, pages 6 and 7) that "[i]t is improper to limit structural apparatus claims to any particular method of making the apparatus, and that it is equally improper to require that the claims be limited to the specific embodiments disclosed in the applicant's specification."

The examiner's position (answer, page 3) is that:

The specification describes a technique for fabricating an oxide isolation region which purports to be of a smaller size than standard techniques but provides no teaching of what the degree of improvement might be or how the resultant device compares with other techniques nor is a specific improvement or final size claimed. The specification also shows a method for forming capacitors which purports to increase the effective area using various techniques such as are known in the art but no specific level of improvement is shown or claimed. The specification shows metallization in multiple levels and shows up to four levels while claiming up to five levels but there is no quantitative showing of a specific improvement in device density.

The examiner further asserts (<u>id.</u>, page 4) that claim 8, for example, recites the size of totally unspecified circuitry, which is not enabled by the specification.

The examiner states (id.) that claim 6, for example:

[S]hows 16-17 million memory cells in an area less than  $14~\text{mm}^2$ . This also includes an area of say  $10~\text{mm}^2$  or even 1 mm² or even less. This then is a claim on all future developments which are part of active research now and also any new techniques that might be developed in the future."

The examiner states (<u>id.</u>, pages 4 and 5) that appellants disclose "several methods and their resultant structures which appellant claims to produce improved memory cell density. None of these methods, or any of their corresponding structural manifestations, are recited in the rejected claims.

We note at the outset that an analysis of whether the claims under appeal are supported by an enabling disclosure requires a determination of whether that disclosure contained sufficient information regarding the subject matter of the appealed claims as to enable one skilled in the pertinent art to make and use the claimed invention. The test for enablement is whether one skilled in the art could make and use the claimed invention from the disclosure coupled with information known in the art without undue experimentation. See United States v. Telectronics, Inc., 857 F.2d 778, 785, 8 USPQ2d 1217, 1223 (Fed. Cir. 1988), cert. denied, 109 S.Ct. 1954 (1989); In re Stephens, 529 F.2d 1343, 1345, 188 USPQ 659, 661 (CCPA 1976).

In order to make a nonenablement rejection, the examiner has the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention. See In re Wright, 999 F.2d 1557, 1561-62, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993) (examiner must provide a reasonable explanation as to why the scope of protection provided by a claim is not adequately enabled by the disclosure). A disclosure which contains a teaching of the manner and process of making and using an invention in terms which correspond in scope to those used in describing and defining the subject matter sought to be patented must be taken as being in compliance with the enablement requirement of 35 U.S.C. § 112, first paragraph, unless there is a reason to doubt the objective truth of the statements contained therein which must be relied on for enabling support. Assuming that sufficient reason for such doubt exists, a rejection for failure to teach how to make and/or use will be proper on that See In re Marzocchi, 439 F.2d 220, 223, 169 USPQ 367, 369 (CCPA 1971). As stated by the court in <u>In re Marzocchi</u>, 439 F.2d at 224, 169 USPQ at 370:

it is incumbent upon the Patent Office, whenever a rejection on this basis is made, to explain why it doubts the truth or accuracy of any statement in a supporting disclosure and to back up assertions of its own with acceptable evidence or reasoning which is inconsistent with the contested statement.

> Otherwise, there would be no need for the applicant to go to the trouble and expense of supporting his presumptively accurate disclosure.

In making the determination of enablement, the examiner shall consider the original disclosure and all evidence in the record, weighing evidence that supports enablement against evidence that the specification is not enabling.

Thus, the dispositive issue is whether the appellant's disclosure, considering the level of ordinary skill in the art as of the date of the appellants' application, would have enabled a person of such skill to make and use the appellants' invention without undue experimentation. The threshold step in resolving this issue as set forth, supra, is to determine whether the examiner has met his or her burden of proof by advancing acceptable reasoning consistent with a lack of enablement.

We turn to the examiner's assertion that the specification shows metallization in multiple levels and shows up to four levels while claiming up to five levels. The examiner is not specific as to which claim or claims is being referred to. We find that the term "metallization" does not appear in any of the claims on appeal, and presume the examiner is referring to the claimed "at least five conductive line layers" (claims 9 and 10). We note that specification (e.g., page 33) refers to the embodiment of figures 34 and 35 as being "fabricated to include

five composite conductive line layers." In addition, we note that the language "at least five composite conductive line layers" appears in claims 9 and 10 as originally filed.

With respect to the examiner's assertion that the undisclosed circuits of claim 8 are not enabled, we note that the pitch and periphery circuitry and their components are described in the specification (e.g., pages 33, 34, and 38). The examiner fails to set forth specific reasons as to why the combined size of the circuitry and the memory arrays is considered to be nonenabling.

With respect to the examiner's assertion that the disclosed methods or their corresponding structural manifestations are not recited in the claims, we agree with appellants (brief, page 22) that the claims are directed to "a new device not previously produced, not a particular method for making it." We note that appellant has disclosed plural embodiments, and the examiner (Paper No. 8, mailed December 23, 1996) required an election of species. We find no language in the disclosure, and none has been brought to our attention by the examiner, that would confine appellants' claims to the specific disclosed embodiments.

With regard to the examiner's assertion that the specification provides no teaching of what the degree of

improvement might be, we make reference to pages 16 and 17 of the brief, where appellants point to methods and techniques disclosed in the specification for achieving the specific densities claimed. These include reducing bird's beak encroachment, maximizing memory storage cell charge storage capacity, reducing mask misalignment spacing between adjacent devices, using a comparatively large number of conductive line layers to take advantage of the elimination of field oxide regions between certain adjacent memory cells, and bit line circuitry requirements and associated bit line spacing using a vertical three level twist or swap design achieving equal bit line lengths running on the upper and lower levels of the design.

In addition, we find that the specific device densities achieved are found in the specification. For example, the specification recites (page 37) that at the 16M memory cell integration level, a total of no more that 17,000,000 (typically 16,777,216) functional and operably addressable memory cells are provided by the multiple memory arrays 160, and that the occupied area of all of the functional and operably addressable memory cells on the die will have a total combined area which is no greater than 14mm<sup>2</sup>.

With regard to the examiner's assertion that a specific improvement or final size is not claimed, we note that claim 6, for example, recites "a total of from 16,000,000 to 17,000,000 functionally and addressable memory cells . . . on the die having a total combined area which is no greater than 14 mm²" has basis in the specification, as discussed, supra and sets forth a specific improvement. In addition, we observe that the language regarding device density found in the claims on appeal is very similar to the language of the originally filed claims.

Appellants rely upon the statement in <u>In re Fischer</u>, 427 F.2d 833, 839, 166 USPQ 18, 24 (CCPA 1970) that:

It is apparent that such an inventor should be allowed to dominate the future patentable inventions of others where those inventions were based in some way on his teachings. Such improvements, while unobvious from his teachings, are still within his contribution, since the improvement was made possible by his work. equally apparent, however, that he must not be permitted to achieve this dominance by claims which are insufficiently supported and hence not in compliance with the first paragraph of 35 U.S.C. 112. That paragraph requires that the scope of the claims must bear a reasonable correlation to the scope of enablement provided by the specification to persons of ordinary skill in the art. In cases involving predictable factors, such as mechanical or electrical elements, a single embodiment provides broad enablement in the sense that, once imagined, other embodiments can be made without difficulty and their performance characteristics predicted by resort to known scientific laws. In cases involving unpredictable factors, such as most chemical reactions and physiological activity,

the scope of enablement obviously varies inversely with the degree of unpredictability of the factors involved.

From our review of the specification, as discussed, supra, with respect to the aspects of the invention that result in the claimed density, we find a reasonable correlation between the language in the claims and the enablement of the disclosure with respect to the specific claim language (e.g., claim 22) relating to appellants achieving a density of at least 128 of the functional and operable addressable memory cells within an area of 100 square microns.

This brings us to the examiner's assertion (answer, pages 4 and 5) that the scope of enablement is not commensurate with the scope of the protection sought by appellants because of the openended language found in the claims. The examiner asserts that the recitation in claim 6 (<u>id.</u>, page 4) that the 16,000,000 to 17,000,000 memory cells are in an area less that 14 mm², "also includes an area of 10 mm² or even 1 mm² or even less," and that this is a claim on all future developments which are part of active research now." The examiner further asserts (<u>id.</u>, page 5) that:

The Federal Circuit has repeatedly held that "the specification must teach those skilled in the art how to make and use the full scope of the claimed invention without 'undue experimentation'." In re Wright, 27 USPO2d 1510, 1513 (Fed. Cir. 1993). With respect to

the breadth of a claim relevant to enablement, the dispositive issue is whether the scope of enablement provided to one skilled in the art by the disclosure is commensurate with the scope of the protection sought by the claims. <u>In re Moore</u>, 169 USPQ 236, 239 (CCPA 1971).

The determination of the propriety of a rejection based upon the scope of a claim relative to the scope of the enablement involves two stages of inquiry. The first is to determine how broad the claim is with respect to the disclosure. The entire claim must be considered. The second inquiry is to determine if one skilled in the art is enabled to make and use the entire scope of the claimed invention without undue experimentation. (MPEP 2164.08)

The scope of applicant's claims includes all semiconductor memory devices of the type claimed, having memory cell density equal to or greater than that achieved by applicant and made through any means at all.

The examiner concludes (id., page 6) that

Applicant may be entitled to a patent because no prior artisan has been able to produce the device produced by applicant. However, applicant's claims may not be so broad so as to include within their scope devices which are not enabled by applicant's disclosure.

Appellant responds (brief, page 18) that "[t]he appellants' claims cannot cover 'all future improvements in density' since the applicable patent term cannot extend more than 20 years from the application filing date, plus any term extensions to which appellants may be entitled." From this statement of appellants, we find that appellants consider the scope of the claims to cover

all increases in density (within the parameters of the claim as a whole) throughout the term of the patent.

In Enzo Biochem, Inc. v. Calgene, Inc., 188 F.3d 1362, 52 USPQ2d 1129 (Fed. Cir. 1999) the court stated that "[t]o be enabling, the specification of a patent must teach those skilled in the art how to make and use the full scope of the claimed invention without 'undue experimentation.'"

Factors for determining enablement are set out in In re Wands, 858 F.2d 731, 8 USPQ2d 1400 (Fed. Cir. 1988). Factors to be considered in determining whether a disclosure would require undue experimentation include (1) the quantity of experimentation necessary, (2) the amount of direction or guidance presented, (3) the presence or absence of working examples, (4) the nature of the invention, (5) the state of the prior art, (6) the relative skill of those in the art, (7) the predictability or unpredictability of the art, and (8) the breadth of the claims. See In re Wands, 858 F.2d at 737, 8 USPQ2d at 1404, citing Ex parte Forman, 230 USPQ 546, 547 (Bd. Pat. App. & Int. 1986). We agree with appellants (brief, page 15) that factors such as breadth of the disclosure and predictability of the art are important factors in determining how far an applicant's claim scope may reasonably extend given the disclosure at the time of the patent application.

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In order to meet his or her initial burden of establishing a prima facie case of lack of enablement based upon the open ended language found in the claims, the examiner would need to show that undue experimentation would be required to meet "the full scope of the claims," due to the presence of the open ended claim language. To establish that undue experimentation would be required to meet the open-ended claim language, the examiner would need to use relevant factors set out in Wands to place in doubt the objective truth of the statements contained in the specification; i.e., that undue experimentation would be needed to make and use the disclosed densities that fall within the full scope of the claims. This the examiner has not done. We note that not all factors need to be considered in each case, since what is relevant depends on the facts of each case. However, we find that the examiner has not presented an analysis of why, for example, the examiner believes that the disclosed invention would require undue experimentation to in order to provide 16 - 17 million memory cells in an area of 10 mm2 (to use the example given by the examiner (answer, page 4). The examiner provides no persuasive argument or convincing line of reasoning that would create doubt that the enabled manufacturing techniques such as reduction of bird's beak encroachment, mask misalignment,

increased numbers of conductive line layers, etc., would result in density within the full scope of the claims, without undue experimentation. Accordingly, we find that the examiner has failed to establish a <u>prima facie</u> case of non-enablement of the claims. The rejection of claims 6-10, 18, 19, 22, 23, 25, and 26 under 35 U.S.C. § 112, first paragraph is therefore reversed.

We turn next to the rejection of claims 6-10, 18, 19, 22, 23, 25, and 26 under 35 U.S.C. § 103 as unpatentable over the admitted prior art considered with Denboer. The examiner's position (answer, pages 6-8) is that appellants admit in the Background of the Invention, that DRAM chips exist in the prior art; that DRAM chips are normally arranged in multiple repeating memory arrays, and that maximizing density of single transistor and other memory cells is a continuing goal in semiconductor memory fabrication. The examiner relies upon Denboer for a teaching of minimizing device size, and use of five conductive layers. According to the examiner (id., page 7) "[i]t would have been obvious to make 16M DRAM chips with ever increasing density . . . because maximizing density is a continuing goal of the art." The examiner adds (id.) that "since applicant discloses that one way to achieve the claimed structure is through the use of at least five conductive layers and since Denboer teaches the

known use of such a structure, the examiner maintains that one skilled in the art would be able to produce the claimed structure."

Appellants assert (brief, page 25), that Denboer is nonenabling because it is a survey report on microprocessor designs. Appellants further assert (id.) that there is no disclosure in Denboer indicating that appellants' claimed density had been achieved or would have even been possible. Appellants further assert (id., page 26) that the examiner cannot use appellants' specification for evidence of how to use five conductive layers to produce 16M chips of the claimed density, as (id.) "appellants' own novel disclosure is not 'prior art' as to the appellants."

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive

at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole. See id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPO 685, 686 (Fed. Cir. 1986); <u>In re Piasecki</u>, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and <u>In re</u> Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

At the outset, we find that appellants have not provided sufficient evidence to establish that Denboer is nonenabling. In Denboer, the IBM PC601 chip is disclosed as being a 50 MHz, 64 bit RISC device. The package is described as die-mounted, flip-

chip style, on a thin ceramic substrate. The technology die size, die area, number of metal levels, number of poly areas, interlevel connect, minimum gate size are disclosed in Table 1. In addition, Denboer discloses that the epitaxial silicon and CMOS process results in a 6 transistor cache RAM cell. Denboer further discloses the results achieved from the chemical-mechanical planarization technique, etc. Denboer further shows photographs of a cross section of a chip. The mere fact, alone, that Denboer is directed to a survey article is insufficient to show lack of enablement of the reference, particularly in view of the high degree of predictability in the electrical and mechanical arts.

As to the examiner's use of appellants' disclosure of the use of five conductive line layers in achieving the claimed densities, we agree with appellants that it is improper for the examiner to use appellants' invention as evidence of how to use the five conductive layers of Denboer to produce the 16M chips of the claimed densities. In addition, even though Denboer discloses five metallization levels and a gate length of  $<0.5\mu\text{m}$ , we find no suggestion in Denboer of the claimed density. The examiner's statement (answer, page 7) that it would have been obvious to make 16M chips with "ever increasing device density"

does not address the specific densities recited in the claims. While Denboer uses five metallization levels and discloses a gate size of  $<0.5\mu\text{m}$ , it does not necessarily follow that the claimed density would result. The examiner has not pointed to any teaching or suggestion in the Admitted Prior Art or Denboer, nor are we aware of any teaching or suggestion, that would have lead an artisan to conclude that the combined teachings of the Admitted Prior Art and Denboer would have resulted in the claimed densities.

The examiner may not resort to speculation or unfounded assumptions to supply deficiencies in establishing a factual basis. See In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967). Stated differently, the subjective opinion of the examiner as to what is or is not obvious, without evidence in support thereof, does not provide a factual basis upon which the legal conclusion of obviousness can be reached. We therefore find that the examiner has failed to establish a prima facie case of obviousness of the claimed invention. Accordingly, the rejection of claims 6-10, 18, 19, 22, 23, 25, and 26 under 35 U.S.C. § 103(a) is reversed.

#### CONCLUSION

To summarize, the decision of the examiner to reject claims 6-10, 18, 19, 22, 23, 25, and 26 under 35 U.S.C. § 112, first paragraph, is reversed. The decision of the examiner to reject claims 6-10, 18, 19, 22, 23, 25, and 26 under 35 U.S.C. § 103 is reversed.

# REVERSED

✓ JOSEPH F. RUGGIERO

Administrative Patent Judge

JOSEPH L. DIXON

Administrative Patent Judge

STUART S. LEVY

Administrative Patent Judge

BOARD OF PATENT APPEALS

AND

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